



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/537,661

06/06/2005

Masaharu Ito

8017-1170

5474

466 7590 04/14/2009
YOUNG & THOMPSON
209 Madison Street
Suite 500
ALEXANDRIA, VA 22314

EXAMINER

LE, DINH THANH

ART UNIT

PAPER NUMBER

2816

MAIL DATE

DELIVERY MODE

04/14/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/537,661	Applicant(s) ITO ET AL.	
	Examiner DINH T. LE	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 February 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 25-30, 32-35, 38, 39, 41, 42, 44 and 45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 25-30, 32-35, 38-39, 41-42 and 44-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

NON-FINAL REJECTION

The rejection under 35 USC, 112 second paragraph, has been withdrawn in view of the amendments to the claims.

The new prior art reference necessitated a new ground of rejection as below:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 25-30, 32-35, 38-39, 41-42 and 44-45 are rejected under 35 USC 103 (a) as being unpatentable over Figure 1 of the admitted prior art in view of Shino et al (JP2000-228602) and further in view of Higgins et al (US 5,373,264).

Regarding claims 25, 28 and 38-39, the admitted prior art discloses in Figure 1 a circuit comprising:

- transistor (FET 101);
- distributed lines (102d, 103,104) being coupled to the transistor (101); and
- a bias power source (Vg) for supplying said gate with a predetermined DC voltage.

However, the admitted prior art fails to suggest that the distributed line (102d) comprise two parallel lines and a resistor or a capacitor coupled between an output terminal and ground for

Art Unit: 2816

adjusting the negative resistance value

Nevertheless, Shino et al suggest in Figures 1-4 an inductor comprising two parallel lines (4- 5) for facilitating frequency regulation, see the Abstract.

Higgins, Jr. suggests in Figures 1- 4 to connect a capacitor (28a, 28b, 40a, 40b) and inductor (16', 26) between one terminal of the transistor (12) and ground for adjusting the negative resistance value.

It would have been obvious to a person having skill in the art at the time the invention was made to replace the line (102d) of the admitted prior art with two parallel lines as suggested by Shino et al for the purpose of facilitating frequency regulation, and employ the capacitor and inductor as suggested by Higgins, Jr. in the modified circuit of the admitted prior art for the purpose of adjusting the negative resistance value.

Regarding claims 26-27, 29-30 and 32-35, since the modified circuit of the admitted prior art is a high frequency circuit, all components such as inductors and capacitors would be formed with the distributed lines and the dimension of the lines determines the capacitance and inductance values. Thus, selecting the length and width for the lines as claimed is considered to be a matter of a design expedient for an engineer depending upon the particular application in which the circuit of the admitted prior art is to be used. Lacking of showing any criticality, it would have been obvious to a person having skill in the art at the time the invention was made to select the length for the lines of the modified circuit of the admitted prior art as claimed for the purpose of providing a predetermined inductance value in order to accommodate with a frequency plan of a predetermined system.

Regarding claims 41-42 wherein a resistor (117) is connected to a DC voltage (Vd) in Figure 1 of the admitted prior art for biasing the transistor (101).

Regarding claims 44-since the circuit of the admitted prior art is used in a predetermined filter circuit it inherently connected to a resonator of the predetermined filter circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan, can be reached at (571) 272-1988.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DINH T. LE/

Primary Examiner, Art Unit 2816